

SHRAVANI SHRIRAMWAR

☎ 8329051018 |

✉ Shriramwarshravani@gmail.com |

🌐 www.linkedin.com/in/shravani-shriramwar

EDUCATION

Vellore Institute of Technology

Masters of Technology (MTECH) – VLSI Design- **GPA: 7.64/10**

August 2021 – May 2023

Chennai, India

Pune Vidyarthi Griha

Bachelor of Engineering (B.E.) – Electronics and Telecommunications – **GPA: 7.66/10**

July 2016 – June 2020

Pune, India

INDUSTRY EXPERIENCE

Truminds Software Systems

Embedded Software Engineer

March 2025-Present

- Contributing to the development and optimization of **Linux-based system-level** applications using **C programming**, with a focus on performance tuning and debugging.
- Collaborating with cross-functional teams to enhance software scalability and system architecture, ensuring solutions meet client requirements.

Alstom

Project Intern- ETCS Department

September 2022 – June 2023

Bengaluru, India

- Drove design, development, and verification of safety-critical embedded software for train signaling systems, adhering to industry standards using **Embedded C** and **Cadence Virtuoso**.
- Mastered advanced software development methodologies and **verification protocols** to ensure functional integrity in mission critical environments.

TRAINING EXPERIENCE

Vector India

Apprenticeship – Embedded Systems

March 2024 – December 2024

Hyderabad, India

- Engineered embedded systems using **C**, **C++**, and **Embedded C** across **8051** and **ARM7** architectures, integrating peripherals via **UART**, **SPI**, **I2C** and **CAN** interfaces for real-time, low latency communication.
- Architected robust solutions leveraging **RTOS** for multitasking while optimizing data flow across **TCP/IP** networks on **LINUX** platforms.
- Leading the way in performance optimization using low level hardware-software interface, sophisticated **DSA** techniques and system debugging to guarantee effective resource use and scalability.

TECHNICAL SKILLS

Programming Languages – C, C++, Embedded C

HDL Language – Verilog, System Verilog, UVM

Scripting – Python, Perl, TCL-Tk

Microcontroller – Microcontroller 8051, ARM- LPC 2129

Communication Protocol – TCP/IP, I2C, SPI, UART, CAN

Operating System – LINUX (for embedded systems and real-time development)

Area of Interest – LINUX Development, Firmware development, Embedded Systems, ARM Architectures

ACADEMIC PROJECTS

ECU Diagnostic System

- Engineered an ECU diagnostic system using **CAN Protocol** to optimize fault detection, reporting, and troubleshooting in automotive environments.
- Developed diagnostic routines for real-time system monitoring and implemented a configurable user interface for executing diagnostic tests and adjusting ECU parameters

Tools used: Keil uVision4, Proteus, ARM2129 kit

Implementation of 16-bit RISC Processor

- Devised a 16-bit RISC processor incorporating a **4-stage pipeline** to optimize instruction throughput and mitigate pipeline stalls.
- Engineered the design to enhance instruction-level parallelism and minimize structural, data and control hazards, employing **VCS** for RTL simulation and **Cadence Virtuoso** for comprehensive circuit level synthesis and validation.

Low power FA by exploring new XOR and XNOR gates using CNTFET Technology

- Synthesized high-efficiency designs for hybrid XOR-XNOR gate-based Full Adders, culminating in the proposal of a novel 18T SRAM-based IMC Full Adder to enhance computational density and minimize latency in arithmetic operations.
- Leveraged comprehensive modeling with **MATLAB** for circuit behavior analysis and **VCS** for exhaustive gate-level simulation

and timing verification, ensuring robust performance under varying operational conditions.

Assertion based Verification of FIFO

- Executed assertion-based verification of a **FIFO design** utilizing **System Verilog**, meticulously developing code for the First In First Out architecture within the **Xilinx** environment.
- Deployed a robust verification ecosystem with **EDA Playground** as a comprehensive checking tool, generating simulation waveforms using **EP Wave** to facilitate in-depth analysis of timing and functional correctness.

Low Power Subthreshold Domino Logic

- Investigated Low Power **Subthreshold Domino Logic** by simulating an **8-input OR gate**, focusing on optimizing energy efficiency and performance at sub-threshold voltage levels.
- Utilized advanced design tools, specifically **Xilinx** for synthesis and **Cadence Virtuoso** for detailed circuit characterization and analysis, ensuring robust functionality under low-power conditions.

VLSI Implementation of Image denoising and Compression algorithms using DCT

- Designed a high-efficiency VLSI architecture for image denoising and compression using **Discrete Cosine Transform (DCT)** with row-column decomposition, optimizing SNR, compression ratio, and MSE.
- Implemented in **Verilog**, validated through **MATLAB** for algorithm optimization, and synthesized using **Xilinx** for hardware simulation and performance verification.

CERTIFICATION

- **Embedded Systems Programming on ARM Cortex-M3/M4 Processor (Udemy), 2024**